Atty. Docket No. OF03P212/US
Serial No: 10/733,884

Amendments to the Claims

Please cancel claim 2 without prejudice, add new claims 6-21, and amend the remaining claims as follows:

1. (Currently Amended) A method of manufacturing a semiconductor device, comprising:

forming a first conductive line on a semiconductor substrate;

forming an insulating layer on the semiconductor substrate and the first conductive line;

etching parts of the insulating layer where a plurality of via holes will be formed to a certain thickness so as not to expose the first conductive line;

selectively etching ~~forming~~ a plurality of via holes in each of said parts of ~~by selectively etching~~ the insulating layer in order to expose the first conductive line;

etching trenches in the insulating layer to a certain thickness;

forming a metal barrier the insulating layer and in the via holes; and

forming a plug by depositing a conductive layer sufficiently to fill the via holes, and then planarizing the conductive layer until the conductive layer is substantially coplanar with the insulating layer.

2. (Cancelled)

3. (Currently Amended) The method of claim 1, ~~wherein said forming a plurality of via holes comprises~~further comprising:

forming a first photoresist pattern on the insulating layer, in order to expose the parts of the insulating layer where the plurality of via holes will be formed;

~~removing the parts of the insulating layer to a certain thickness by etching the parts of the insulating layer,~~ using the first photoresist pattern as an etching mask when etching the parts of the insulating layer;

forming a second photoresist pattern on the insulating layer, in order to expose parts of the insulating layer where each via hole will be formed; and

forming a plurality of via holes by removing the parts of insulating layer where each via hole will be formed enough to expose the first conductive line, by etching the parts of the insulating layer for each via hole using the second photoresist pattern as an etching mask.

4. (Currently Amended) The method of claim 1, ~~wherein said forming trenches comprises~~further comprising:

forming a third photoresist pattern on the insulating layer in order to expose parts of the insulating layer where the trenches will be formed; and

~~forming trenches by removing the parts of the insulating layer where the trenches will be formed to a certain thickness, by etching the parts of the insulating layer for the trenches by~~ using the third photoresist pattern as an etching mask when etching the parts of the insulating layer for the trenches.

5. (Currently Amended) The method of claim 1, wherein the first conductive line ~~and the plug~~ comprises copper.

6. (New) The method of claim 1, wherein the conductive layer and the plug comprise copper.

7. (New) The method of claim 6, wherein forming the plug and depositing the conductive layer comprises depositing a copper seed layer by physical vapor deposition (PVD) and forming a copper bulk layer on the copper seed layer by electroplating.

8. (New) The method of claim 1, wherein forming the first conductive line comprises sputtering a metal layer, patterning the metal layer using photolithography, and etching the metal layer.

9. (New) The method of claim 1, wherein each plurality of via holes has a combined width equal to a width of a corresponding insulating layer part.

10. (New) A method of manufacturing a semiconductor device, comprising:

etching a plurality of via holes in each of a plurality of parts of an insulating layer, each plurality of via holes exposing a conductive line on a semiconductor substrate;

etching trenches in the insulating layer to a certain thickness, each of said trenches enabling electrical connection of a subsequently formed conductive layer through a corresponding plurality of via holes to the exposed conductive line;

forming a metal barrier on the insulating layer and in the via holes and trenches;

depositing a conductive layer in the via holes and trenches sufficiently to fill the via holes and trenches; and

planarizing the conductive layer until the conductive layer is substantially coplanar with the insulating layer.

11. (New) The method of claim 10, wherein the trenches are etched before the plurality of via holes are etched.

12. (New) The method of claim 10, wherein the plurality of via holes has a combined width equal to a width of a corresponding insulating layer part.

13. (New) The method of claim 10, further comprising forming the first conductive line by sputtering a metal layer, patterning the metal layer using photolithography, and etching the metal layer.

14. (New) The method of claim 10, wherein the conductive layer and the plug comprise copper.

15. (New) The method of claim 14, wherein forming the plug and depositing the conductive layer comprises depositing a copper seed layer by physical vapor deposition (PVD) and forming a copper bulk layer on the copper seed layer by electroplating.

16. (New) A semiconductor device, comprising:

a first conductive line on a semiconductor substrate;

an insulating layer on the semiconductor substrate and the first conductive line;

a plurality of via holes in each of a plurality of parts of the insulating layer, each of the plurality of via holes exposing the first conductive line, and each of the parts of the insulating layer other than the via holes having a certain thickness greater than zero but less than the insulating layer thickness;

trenches in the insulating layer having a certain depth;

a metal barrier lining the insulating layer and the via holes; and

a plug and a conductive layer filling the via holes, the conductive layer being substantially coplanar with the insulating layer.

17. (New) The semiconductor device of claim 16, wherein the first conductive line comprises copper.

18. (New) The semiconductor device of claim 16, wherein the conductive layer and the plug comprise copper.

19. (New) The semiconductor device of claim 16, wherein the metal barrier comprises Ti, TiN, Ta or TaN.

20. (New) The semiconductor device of claim 16, wherein the insulating layer comprises silicon oxide (SiO_2).

21. (New) The semiconductor device of claim 16, wherein each of the plurality of via holes has a width equal to a width of a corresponding insulating layer part.